

WHAT IS CLAIMED IS:

1. A leadframe comprising:
a rectangular frame;
a chip pad inside of and integrally connected to the frame; and
a plurality of leads, each said lead including an inner end adjacent to the chip pad,
5 an outer end integrally connected to the frame, a first surface, and a second surface
opposite the first surface,
wherein the second surface of each lead is split into a first region and a second
region by a groove including a horizontal third surface that extends across the lead, the
first region is between the frame and the third surface, and the second region is between
10 the third surface and the inner end of the lead.
2. The leadframe of claim 1, wherein the second surface of each lead includes a
recessed fourth surface that begins at the inner end of the lead and extends toward the
second region.
3. The leadframe as claimed in claim 2, wherein the chip pad includes a first surface,
15 a second surface opposite a central portion of the first surface, and a third surface
opposite a peripheral portion of the first surface and surrounding the second surface,
wherein the third surface is recessed from the second surface.
4. The leadframe of claim 3, wherein the first surface of the chip pad includes a
groove bottomed by a horizontal fourth surface, said groove extending in a ring adjacent
20 to peripheral sides of the chip pad.
5. The leadframe of claim 1, wherein the chip pad includes a first surface, a second
surface opposite a central portion of the first surface, and a third surface opposite a
peripheral portion of the first surface and surrounding the second surface, wherein the
third surface is recessed from the second surface.

6. The leadframe of claim 5, wherein the first surface of the chip pad includes a groove bottomed by a fourth surface, said groove extending in a ring adjacent to peripheral sides of the chip pad.

7. A leadframe comprising:

5 a rectangular frame;

a chip pad inside of and integrally connected to the frame, wherein the chip pad includes a first surface, a second surface opposite a central portion of the first surface, a third surface opposite a peripheral portion of the first surface and surrounding the second surface, said third surface being recessed from the second surface, and the first surface of
10 the chip pad includes a groove bottomed by a horizontal fourth surface, said groove extending in a ring adjacent to peripheral sides of the chip pad; and

a plurality of leads, wherein each said lead includes an inner end adjacent to the chip pad, an outer end integrally connected to the frame, a first surface, and a second surface opposite the first surface, the second surface of the chip pad including a recessed
15 third surface that extends across the lead.

8. The leadframe of claim 7, wherein the recessed third surface bisects the second surface of each lead into a first region and a second region, the first region is between the frame and the third surface, and the second region is between the third surface and the inner end of the lead.

20 9. The leadframe of claim 8, wherein the second surface of each lead includes a recessed fourth surface that begins at the inner end of the lead and extends toward the second region.

10. The leadframe of claim 7, wherein the recessed third surface begins at the inner end of the lead.

25 11. A semiconductor package comprising:

a chip pad having a first surface and an opposite second surface;

a plurality of leads each including an inner end adjacent to the chip pad, an opposite outer end, a first surface, and a second surface opposite the first surface, wherein

the second surface of each lead is split into a first region and a second region by a groove including a horizontal third surface that extends across the lead, the first region is between the outer end of the lead and the third surface, and the second region is between the third surface and the inner end of the lead;

5 a semiconductor chip mounted on the first surface of the chip pad and in an electrical connection with the first surface of at least some of the leads; and

a package body of a hardened encapsulant material over the chip and at least the first surface of the chip pad, wherein the third surface of the leads is covered by the encapsulant material, and the first and second regions of the second surface of the leads
10 are exposed in a plane of a first exterior surface of the package body.

12. The semiconductor package of claim 11, wherein the second surface of each lead includes a recessed fourth surface that begins at the inner end of the lead and extends toward the second region.

13. The semiconductor package of claim 12, wherein the semiconductor chip is
15 electrically connected to the first surface of each said lead by a wire, wherein a point of connection of the wire and the first surface of the lead is opposite the second region of the lead outward of the fourth surface.

14. The semiconductor package of claim 11, wherein the second surface of the chip pad is opposite a central portion of the first surface of the chip pad; and
20 the chip pad includes a third surface opposite a peripheral portion of the first surface and surrounding the second surface, wherein said third surface is recessed from the second surface and covered by said encapsulant material, and the second surface of the chip pad is exposed in the plane of the first exterior surface of the package.

15. The semiconductor package of claim 14, wherein the first surface of the chip pad
25 includes a groove bottomed by a fourth surface, said groove extending in a ring adjacent to peripheral sides of the chip pad, at least one conductive wire is electrically connected between the semiconductor chip and the fourth surface within the groove, and the groove is filled with said encapsulant material.

16. A semiconductor package comprising:

a chip pad including first surface, a second surface opposite a central portion of the first surface, and a third surface opposite a peripheral portion of the first surface and surrounding the second surface, said third surface being recessed from the second surface, wherein the first surface of the chip pad includes a groove bottomed by a fourth surface;

a plurality of leads, wherein each said lead includes an inner end adjacent to the chip pad, a first surface, and a second surface opposite the first surface, and the second surface of the lead includes a recessed horizontal third surface that extends across the lead;

a semiconductor chip mounted on the first surface of the chip pad and in an electrical connection with the first surface of at least some of the leads and with the fourth surface of the chip pad within the groove; and

a package body of a hardened encapsulant material over the chip, over the first, third, and fourth surfaces of the chip pad, and over the third surface of the leads, wherein the second surface of the chip pad and the third surface of the leads are exposed in a plane of a first exterior surface of the package body.

17. The semiconductor package of claim 16, wherein the groove in the first surface of the chip pad surrounds the chip.

18. The semiconductor package of claim 16, wherein the recessed third surface of the lead splits the second surface of each lead into a first region and a second region, the first region is between a peripheral side of the package body and the third surface, and the second region is between the third surface and the inner end of the lead.

19. The semiconductor package of claim 18, wherein second surface of each lead includes a recessed fourth surface that begins at the inner end of the lead and extends toward the second region.

20. The semiconductor package of claim 16, wherein the recessed third surface begins at the inner end of the lead.

09045601.042701